WHAT IS CLAIMED IS:

1. An image sensor comprising:

a semiconductor substrate of a first conductivity type;

a peripheral circuit formed on a first region of the semiconductor substrate, wherein a ground voltage level is applied to the first region;

a unit pixel array having a plurality of unit pixels formed on a second region of the semiconductor substrate, wherein the first region is isolated from the second region and wherein a negative voltage level is applied to the second region; and

a negative voltage circuit configured to provide the negative voltage for the second region.

2. The image sensor as recited in claim 1, wherein the image sensor comprises a buried layer isolating each of the unit pixels so that the buried layer surrounds the unit pixels.

3. The image sensor as recited in claim 2, wherein the semiconductor substrate comprises a P^+-type substrate and a P-type epitaxial layer which is formed on the P^+-type substrate, wherein the buried layer is formed in the P-type epitaxial layer.

4. The image sensor as recited in claim 3, wherein the negative voltage circuit comprises a P^+ diffusion layer which is formed in the P-type epitaxial layer and wherein the negative voltage is applied to the P^+ diffusion layer.

5. The image sensor as recited in claim 4, wherein the P^+ diffusion layer is shared with the second region of neighboring pixels.

6. An image sensor, comprising:

a plurality of unit pixels formed in a first region of a substrate that is biased at a ground reference, each pixel surrounded by a first epitaxial layer that is biased at a negative potential relative to the ground reference; and

a bias generator formed in a second region of the substrate that is biased to the ground reference.

7. An image sensor, comprising:

a substrate having a first conductivity type;

a plurality of unit pixels formed in a first region of the substrate; and

a peripheral circuit formed in a second region of the substrate, the peripheral circuit operable to generate a negative voltage relative to a ground reference, wherein the first region is biased at the negative voltage and the second region is biased at the ground reference.

8. The image sensor of claim 7, wherein the first and second regions have a second conductivity type.

9. The image sensor of claim 7, wherein each unit pixel comprises a photodiode that is reverse biased at the negative voltage.

10. The image sensor of claim 9, wherein each unit pixel further comprises:

a transfer transistor having a gate controlled by a transfer signal, a source coupled to the photodiode, a body biased at the negative voltage and a drain coupled to a sense node.

11. The image sensor of claim 10, wherein each unit pixel further comprises a capacitor having a first end coupled to the sense node and a second end coupled to the negative voltage.

12. The image sensor of claim 11, wherein each unit pixel further comprises a reset transistor having a gate controlled by a reset signal, a source coupled to the sense node, a drain coupled to a positive power supply and a body biased at the negative voltage.

13. The image sensor of claim 12, wherein each unit pixel further comprises a drive transistor having a gate coupled to the sense node, a drain coupled to the positive power supply, a body biased at the negative voltage and a source.

14. The image sensor of claim 13, wherein each unit pixel further comprises a select transistor having a gate controlled by a select transistor, a drain coupled to the source of the drive transistor, a body biased at the negative voltage and a source embodying an output of the unit pixel.

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15. A method of improving the charge transfer efficiency of a photodiode device, the method comprising the steps of:

providing a ground reference;

providing a bias generator for generating a negative potential relative to the ground reference; and

providing a photodiode device having a photodiode including a p-type side that is electrically coupled to the negative potential.